IN THE CLAIMS

1. (Currently amended) Phase detector for detecting a phase between a first input signal and a second input signal, ~~characterized in that said phase detector comprises~~ comprising:
a subtracting circuit ~~or~~ for subtracting a first signal derived from a first one of the input signals from a second signal derived from a second one of the input signals to form a result signal representing an arithmetic difference between the first and second signals;
an arithmetic operation circuit responsive to the result signal for forming multiple ~~establishing~~ differences ~~between said input~~ signals; and ~~comprises~~
a selector for selecting one of said difference signals to be an output signal.

2. (Currently amended) Phase detector according to claim 1, ~~characterized in that~~wherein said selector is a feedbackless selector.

3. (Currently amended) Phase detector according to claim 2, ~~characterized in that~~wherein said selector comprises latches clocked by said second input signal and for receiving said first input signal and for generating latch signals and comprises a multiplexer controlled by said second input signals and for receiving said latch signals and for generating a selection signal.

4. (Currently amended) Phase detector according to claim 1, ~~characterized in that~~wherein said phase circuit comprises a converter for converting said input signals into compensated input signals.

5. (Currently amended) Phase detector according to claim 4, ~~characterized in that~~wherein said converter comprises per input signal a buffer circuit coupled to a replica circuit.

6. (Currently amended) Phase detector according to claim 4, ~~characterized in that~~wherein said ~~difference establisher comprises a~~ subtracting circuit ~~for subtracting~~subtracts compensated input signals from each other ~~and~~ to generating thea result signal, and the arithmetic operation circuit comprises a modulus circuit for generating moduli of said

result signal, with said phase detector comprising a multiplexer to be controlled by a selection signal for selecting a modulus.

7. (Currently amended) Phase detector according to claim 4, ~~characterized in that~~wherein said subtracting circuit subtracts compensated input signals from each other to generating the result signal, and the arithmetic operation circuit~~difference establisher comprises a subtracting circuit for subtracting compensated input signals from each other and generating a result signal and~~ comprises a squaring circuit for generating squares of said result signal, with said phase detector comprising a multiplexer to be controlled by a selection signal for selecting a square.

8. (Currently amended) Phase Locked Loop comprising a phase detector for detecting a phase between a first input signal and a second input signal, ~~characterized in that~~ said phase detector comprises: a subtracting circuit for subtracting a signal derived from one of the input signals from a signal derived from another of the input signals to form a result signal;
an arithmetic operation circuit responsive to the result signal for forming multiple difference signals; and
a selector for selecting one of said difference signals to be an output signal.~~comprises a subtractor for establishing differences between said input signals and comprises a selector for selecting one of said differences to be an output signal~~.

9. (Currently amended) Method for detecting a phase between a first input signal and a second input signal, ~~characterized in that~~wherein said method comprises the step of,
subtracting a signal derived from one of the input signals from a signal derived from another of the input signals to form a result signal;
responsive to the result signal, forming multiple difference signals; and
selecting one of said difference signals to be an output signal.~~using a subtractor, establishing differences between said input signals and the step of selecting one of said differences to be an output signal.~~

10. (Canceled)

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